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EXAMINER	
ELPENORD, CANDAL	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,442	BELOTSERKOVSKY ET AL.	
	Examiner	Art Unit	
	CANDAL ELPENORD	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *30 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *January 31, 2005, June 23, 2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

2. Claims 1-4, 9, 13-16, 18-20 have been amended.

The Applicant claimed feature “shared buffer” is treated by the Examiner as storage element that is shared or common by /to multiple network elements.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claims 1, 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al (US 6,247,034 B1) in view of Park et al (US 6,470,030 B1).

Regarding claim 1, Nakai '034 discloses an Orthogonal Frequency Division Multiplexing (OFDM) receiver that is adapted to receive OFDM signals (see, “OFDM receiver for demodulating signals", col. 5, lines 48-57, fig. 1, OFDM Receiver), the OFDM receiver (see, “OFDM receiver for demodulating signals", col. 5, lines 48-57, fig. 1, OFDM Receiver) comprising: a shared buffer that stores data corresponding to the OFDM signals (see, “RAM for storing OFDM symbols wherein the symbols corresponds to unit of data”, 44-51); a processor (see, FFT processor for performing Fast Fourier transform on the stored data in the RAM ", col. 4, lines 44-60) that is adapted to receive data from the shared buffer (see, FFT processor for performing Fast Fourier transform on the stored data in the RAM ", col. 4, lines 44-60), perform computations on the data (see, FFT processor for performing Fast Fourier transform on the stored data in the RAM ", col. 4, lines 44-60) and return data to the shared buffer (see, storing the processed data (i.e. resultant data) from the FFT processor in the RAM, col. 4, lines 8-27, col. 5, lines 6-25).

Regarding claim 13, Nakai '034 discloses a device (see, "OFDM receiver for demodulating signals", col. 5, lines 48-57), comprising: a shared buffer that stores data corresponding to signals (see, "RAM for storing OFDM symbols wherein the symbols corresponds to unit of data", 44-51); a processor that is adapted to receive data from the shared buffer (see, FFT processor for performing Fast Fourier transform on the stored data in the RAM ", col. 4, lines 44-60), perform computations on the data and return data to the shared buffer (see, FFT processor for performing Fast Fourier transform on the stored data in the RAM ", col. 4, lines 44-60, see, storing the processed data (i.e. resultant data) from the FFT processor in the RAM, col. 4, lines 8-27, col. 5, lines 6-25).

Nakai '084 discloses all the claimed limitations with the exception of being silent about the claimed features:

Regarding claim 1, an equalizer module an equalize module that is adapted to receive the data from the shared buffer and equalize the data.

Regarding claim 13, an equalizer module, an equalize module that is adapted to receive the data from the shared buffer and equalize the data, and a device controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module.

However, Park '030 from the same field of endeavor discloses the above claimed features:

Regarding claim 1, an equalizer module (fig. 1, Equalizing Section 600), an equalize module that is adapted to receive the data from the shared buffer and equalize

the data (fig. 1, see Equalizing Section 600 for equalizing data (i.e. pilot signals) received from the memory unit 720, col. 3, lines 57 to col. 4, lines 20, see "performs equalization for compensated channel distortion", recited in col. 4, lines 9-21).

Regarding claim 13, an equalizer module (fig. 1, Equalizing Section 600), an equalize module that is adapted to receive the data from the shared buffer and equalize the data (fig. 1, see Equalizing Section 600 for equalizing data (i.e. pilot signals) received from the memory unit 720, col. 3, lines 57 to col. 4, lines 20, see "performs equalization for compensated channel distortion", recited in col. 4, lines 9-21), and a device controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module (fig. 1, Controller 570 for the controlling access to the memory unit, the FFT processor 710 and the Equalizer element 600, col. 64 to col. 4, lines 8).

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching features of Nakai '034 by using features as taught by Park '030 in order to provide precise OFDM demodulation using common memory element as suggested in col. 2, lines 9-15.

7. **Claims 2, 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al (US 6,247, 034 B1) in view of Park et al (US 6,470,030 B1) as applied to claim 1, 13 above and further in view of Wilson et al (US 7,027,540 B2).

Nakai '034 and Park '030 disclose all the claimed limitations as set forth above with the exception of being silent about claimed features:

Regarding claim 2, a pilot frame tracking module that is adapted to move an FFT window location by changing an index pointer to the shared buffer.

Regarding claim 14, a pilot frame tracking module that is adapted to move an FFT window location by changing an index pointer to the buffer.

However, Wilson et al. in a similar field of endeavor discloses the following features:

Regarding claim 2, a pilot frame tracking module (fig. 5, Tracking Sub-block, recited in col. 8, lines 16-47) that is adapted to move (see "the FFT window position being adjusted", recited in col. 7, lines 58-67) an FFT window location by changing("offsetting FFT window position", recited in col. 6, lines 37-57) an index pointer to the shared buffer (fig. 2-3, Buffer start and FFT buffer end, recited in col. 5, lines 18-32 and col. 6, lines 37-57).

Regarding claim 14, a pilot frame tracking module (fig. 5, Tracking Sub-block, recited in col. 8, lines 16-47) that is adapted to move (see "the FFT window position being adjusted", recited in col. 7, lines 58-67) an FFT window location (see "the FFT window position being adjusted", recited in col. 7, lines 58-67) by changing ("offsetting FFT window position", recited in col. 6, lines 37-57) an index pointer ("adjusting of FFT window position", recited in col. 7, lines 58-67) to the shared buffer (fig. 2-3, Buffer start and FFT buffer end, recited in col. 5, lines 18-32 and col. 6, lines 37-57).

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Nakai '034 with Park '030 by using features as taught by Wilson et al. in order to provide a signal quality that is

reflective of the OFDM data after it has been processed as suggested in col. 2, lines 6-27 for motivation.

8. **Claims 3, 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al (US 6,247, 034 B1) in view of Park et al (US 6,470,030 B1), as applied to claims 1, 13 above, and further in view of Crawford et al (US 6,549,561 B2).

Nakai '034 and '030 disclose the OFDM receiver as set forth above with the exception of being silent about the claimed features:

Regarding claim 3, a pilot carrier tracking module adapted to provide pilot carrier tracking data to the buffer; and a fine carrier estimation module that is adapted to access the buffer to obtain the pilot carrier tracking data.

Regarding claim 15, a pilot carrier tracking module adapted to provide pilot carrier tracking data to the buffer; and a fine carrier estimation module that is adapted to access the buffer to obtain the pilot carrier tracking data.

However, Crawford '561 from the same field of endeavor discloses the above claimed features:

Regarding claim 3, a pilot carrier tracking module ("determining pilot reference points for plurality of pilots", recited in col. 2, lines 45-55) adapted to provide pilot carrier tracking data to the buffer (fig. 4, Storage 308, recited in col. 9, lines 1-7, "reference point storage", recited in col. 2, lines 45-55); and a fine carrier estimation module (fig. 4, Quality Estimator 408, "calculate measure of pilot tracking", recited in col. 14, lines 31-

44) that is adapted to access the shared buffer (fig. 4, Storage 308, recited in col. 9, lines 1-7, "reference point storage", recited in col. 2, lines 45-55) to obtain the pilot carrier tracking data ("OFDM data", recited in col. 6, lines 44-67).

Regarding claim 15, a pilot carrier tracking module ("determining pilot reference points for plurality of pilots", recited in col. 2, lines 45-55) adapted to provide pilot carrier tracking data to the buffer (fig. 4, Storage 308, recited in col. 7, lines 1-7, "reference point storage", recited in col. 2, lines 45-55); and a fine carrier estimation module (fig. 4, Quality Estimator 408, "calculate measure of pilot tracking", recited in col. 14, lines 31-44) that is adapted to access the shared buffer (fig. 4, Storage 308, recited in col. 9, lines 1-7, "reference point storage", recited in col. 2, lines 45-55) to obtain the pilot carrier tracking data ("OFDM data", recited in col. 6, lines 44-67).

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Nakai '034 with Park '030, by using features as taught by Crawford '561 in order to provide transmission quality by tracking OFDM pilot signals as suggested in col. 2, lines 12-34 for motivation.

9. **Claims 4-12, 16-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al (US 6,247,034 B1) in view of Park et al (US 6,470,030), as applied to claims 1, 13 above, and further in view of Rafie et al (US 6,628, 70 B2), Yamada et al (US 2002/0051478 A1), and Scarpa et al (US 2004/0001563).

Regarding claim 4-12, 20, Nakai '034 discloses the OFDM receiver as set above in the method and device.

Regarding claim 6, Park '030 discloses, discloses the equalizer module as recited in above paragraphs, a fine frame synchronization module(fig. 1, Equalizing 600, recited in col. 3, lines 44-56).

Regarding claim 7, Park '030 discloses a fine frame synchronization module ("Frame synchronization algorithm and Fine synchronization", recited in col. 8, lines 18- col. 9, lines 66) that is adapted to exchange data with the buffer ("stored in to memory", recited in col. 8, lines 18-67); a fine frame synchronization module ("Frame synchronization algorithm and Fine synchronization", recited in col. 8, lines 18- col. 9, lines 66) that is adapted to exchange data with the buffer ("stored in to memory", recited in col. 8, lines 18-67).

Regarding claim 8, Park '030 discloses a fine frame synchronization module ("Frame synchronization algorithm and Fine synchronization", recited in col. 8, lines 18- col. 9, lines 66) that is adapted to exchange data with the buffer ("stored in to memory", recited in col. 8, lines 18-67); a fine frame synchronization module ("Frame synchronization algorithm and Fine synchronization", recited in col. 8, lines 18- col. 9, lines 66) that is adapted to exchange data with the buffer("stored in to memory", recited in col. 8, lines 18-67).

Regarding claim 9, Park '030 discloses a coarse carrier estimation (fig. 1, coarse frequency synchronization that calculates an estimated value, recited in col. 4, lines 40-48), a frame synchronization module (fig. 1, Frame Synchronization Section

540, recited in col. 3, lines 44- col. 4, lines 8) that is adapted to exchange data with the buffer (fig. 1, 4, DPRAM 69C, “output samples stored into the memory”, recited in col. 8, lines 19-67).

Regarding claim 10, Park ‘030 discloses a fine frame synchronization module (“Frame synchronization algorithm and Fine synchronization", recited in col. 8, lines 18- col. 9, lines 66) that is adapted to exchange data with the buffer (“stored in to memory”, recited in col. 8, lines 18-67); a fine frame synchronization module (“Frame synchronization algorithm and Fine synchronization", recited in col. 8, lines 18- col. 9, lines 66) that is adapted to exchange data with the buffer(“stored in to memory”, recited in col. 8, lines 18-67).

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching features of Nakai ‘034 by using features as taught by Park ‘030 in order to provide precise OFDM demodulation using common memory element and to compensate for offset in frequency and phase as suggested in col. 2, lines 9-44 for motivation.

Nakai ‘034 and Park ‘030 disclose all the claimed limitations with the exception of being silent with respect to claimed features:

Regarding claim 4, an equalizer tap initialization module (that is adapted to exchange data with the shared buffer; and a least mean squares (LMS) adaptation engine that is adapted to provide input to the equalizer tap initialization module; **regarding claim 5**, the equalizer tap initialization module is adapted to reuse output from the LMS adaptation engine to perform a recursive division algorithm, **regarding**

claim 6, a least mean squares (LMS) adaptation engine that is adapted to provide input to the equalizer module; and wherein the equalizer module is adapted to reuse the data provided by the LMS adaptation engine to compute a least mean squares tap update value, **regarding claim 7**, a least mean squares (LMS) adaptation engine that is adapted to provide input to the fine frame synchronization module, **regarding claim 8**, wherein the fine frame synchronization module is adapted to reuse output from the LMS adaptation engine to perform a recursive division algorithm, **regarding claim 10**, an equalizer tap initialization module that is adapted to exchange data with the shared buffer; **regarding claim 17**, a least mean squares (LMS) adaptation engine that is adapted to provide input to the equalizer module; and wherein the equalizer module is adapted to reuse the data provided by the LMS adaptation engine to compute a least mean squares tap update value.

However, Rafie '707 from the same field of endeavor discloses the above claimed features:

Regarding claim 4, an equalizer tap initialization module ("adaptive equalizer providing initial tap estimates", recited in col. 4, lines 57- col. 5, lines 7) that is adapted to exchange data with the shared buffer (fig. 5, Memory circuit 512, recited in col. 10, lines 10-19, "storing the tap coefficient values", recited in col. 4, lines 57- col. 5, lines 7); and a least mean squares (LMS) adaptation engine (fig. 6, Least Square Mean equalizing operation, recited in col. 11, lines 24-58) that is adapted to provide input (fig. 5, Box 505, providing the input to adaptive equalizer, recited in col. 9, lines 55 –col. 10,

lines 9) to the equalizer tap initialization module ("adaptive equalizer implements LMS algorithm", recited in col. 11, lines 24 - col. 12, lines 9).

Regarding claim 5, an equalizer tap initialization module ("adaptive equalizer providing initial tap estimates", recited in col. 4, lines 57- col. 5, lines 7).

Regarding claim 6, a least mean squares (LMS) adaptation engine (fig. 6, Least Square Mean equalizing operation, recited in col. 11, lines 24-58) that is adapted to provide input (fig. 5, Box 505, providing the input to adaptive equalizer, recited in col. 9, lines 55 –col. 10, lines 9) to the equalizer module ("adaptive equalizer implements LMS algorithm", recited in col. 11, lines 24 - col. 12, lines 9); and wherein the equalizer module (fig. 5, Adaptive Equalizer 503, recited in col. 10, lines 35-49) is adapted to reuse the data provided by the LMS adaptation engine (fig. 6, Least Square Mean equalizing operation, recited in col. 11, lines 24-58) to compute a least mean squares tap update value (fig. 5, Adaptive Equalizer 506, "producing an equalized output signal and tap coefficient values", recited in col. 10, lines 61- col. 11, lines 23).

Regarding claim 7, a least mean squares (LMS) adaptation engine (fig. 6, Least Square Mean equalizing operation, recited in col. 11, lines 24-58) that is adapted to provide input to the fine frame synchronization module ("estimate of carrier phase", recited in col. 14, lines 39-51).

Regarding claim 10, an equalizer tap initialization module ("adaptive equalizer providing initial tap estimates", recited in col. 4, lines 57- col. 5, lines 7) that is adapted to exchange data with the shared buffer (fig. 5, Memory circuit 512, recited in col. 10, lines 10-19, "storing the tap coefficient values", recited in col. 4, lines 57- col. 5, lines 7).

Regarding claim 16, an equalizer tap initialization module ("adaptive equalizer providing initial tap estimates", recited in col. 4, lines 57- col. 5, lines 7) that is adapted to exchange data with the shared buffer (fig. 5, Memory circuit 512, recited in col. 10, lines 10-19, "storing the tap coefficient values", recited in col. 4, lines 57- col. 5, lines 7); and a least mean squares (LMS) adaptation engine that is adapted to provide input (fig. 5, Box 505, providing the input to adaptive equalizer, recited in col. 9, lines 55 –col. 10, lines 9) to the equalizer tap initialization module ("adaptive equalizer providing initial tap estimates", recited in col. 4, lines 57- col. 5, lines 7).

Regarding claim 17, a least mean squares (LMS) adaptation engine (fig. 6, Least Square Mean equalizing operation, recited in col. 11, lines 24-58) that is adapted to provide input (fig. 5, Box 505, providing the input to adaptive equalizer, recited in col. 9, lines 55 –col. 10, lines 9) to the equalizer module ("adaptive equalizer implements LMS algorithm", recited in col. 11, lines 24 - col. 12, lines 9); and wherein the equalizer module (fig. 5, Adaptive Equalizer 503, recited in col. 10, lines 35-49) is adapted to reuse the data provided by the LMS adaptation engine (fig. 6, Least Square Mean equalizing operation, recited in col. 11, lines 24-58) to compute a least mean squares tap update value (fig. 5, Adaptive Equalizer 506, "producing an equalized output signal and tap coefficient values", recited in col. 10, lines 61- col. 11, lines 23).

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features Nakai '034 with Park '030 by using features as taught by Rafie '707 in order to provide compensation for distorted signals when there are offsets between the receiver and the transmitter so that

transmission performance can be improved as suggested in col. 4, lines 16-30 for motivation.

Nakai ‘034, Park ‘030 and Rafie ‘707 disclose all the claimed limitations with the exception of being silent with respect to the following features: **regarding claim 5**, wherein the equalizer tap initialization module is adapted to reuse output from the LMS adaptation engine to perform a recursive division algorithm, **regarding claim 8**, wherein the fine frame synchronization module is adapted to reuse output from the LMS adaptation engine to perform a recursive division algorithm.

However, Yamada ‘487 from the same field of endeavor discloses the above claimed features:

Regarding claim 5, wherein the equalizer tap initialization module (fig. 7, TAP Parameter Estimator, recited in paragraph 0047, lines 1-30) is adapted to reuse output (fig. 7, Replica Tap signal, recited in paragraph 0050) from the LMS adaptation engine (“ use of Least Mean Square algorithm", recited in paragraph 0047) to perform a recursive division algorithm ("Recursive algorithm to obtain updating coefficient”, recited in paragraph 0047).

Regarding claim 8, wherein the fine frame synchronization module is adapted to reuse output from the LMS adaptation engine (“ use of Least Mean Square algorithm", recited in paragraph 0047) to perform a recursive division algorithm ("Recursive algorithm to obtain updating coefficient”, recited in paragraph 0047).

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Nakai ‘034 with Park ‘030

and Rafie '707 by using features as taught by Yamada '487 in order to improve transmission quality.

Nakai '034, Park '030 and Rafie '707 and Yamada '487 disclose all the claimed limitations with the exception of being silent with respect to the claimed features:

Regarding claim 9, wherein the receiver controller is adapted to allow the coarse carrier estimation and frame synchronization module to access the buffer responsive to receipt of at least a portion of a preamble by the OFDM receiver, **regarding claim 10**, wherein the receiver controller is adapted to allow the equalizer tap initialization module, the fine carrier estimation module and the fine frame synchronization module to access the buffer responsive to receipt of at least a portion of a preamble by the OFDM receiver; **regarding claim 11**, comprising: a pilot carrier tracking module that is adapted to receive data from the equalizer module; a pilot frame tracking module that is adapted to provide data to the shared buffer; and wherein the receiver controller is adapted to activate the equalizer module, the pilot carrier tracking module and the pilot frame tracking module responsive to the receipt of at least a portion of an OFDM signal by the OFDM receiver; **regarding claim 12**, wherein the receiver controller is a state machine; **regarding claim 20**, comprising: a pilot carrier tracking module that is adapted to receive data from the equalizer module; a pilot frame tracking module that is adapted to provide data to the shared buffer; and wherein the receiver controller is adapted to activate the equalizer module, the pilot carrier tracking module and the pilot frame tracking module responsive to the receipt of at least a portion of an OFDM signal by the device.

However, Scarpa '563 from the same field of endeavor discloses the above claimed features:

Regarding claim 9, wherein the receiver controller (fig. 6, Control Modules 1204 with processor 12010, recited in paragraph 0109) is adapted to allow the coarse carrier estimation ("obtaining coarse estimate:, recited in paragraph 0050, fig. 1220, Course Frequency Estimation Module, recited in paragraph 0051) and frame synchronization module (fig. 3, Device 270, "Perform Frequency Correction of OFDM Signal", recited in paragraphs 0040-0043) to access the shared buffer (fig. 6, Memory Block, recited in paragraphs 0109-0110) responsive to receipt ("received OFDM signal", recited in paragraph 0043) of at least a portion of a preamble ("preamble portion", recited in paragraph 0044) by the OFDM receiver (fig. 6, OFDM receiver 1206, recited in paragraph 0109).

Regarding claim 10, wherein the receiver controller (fig. 6, Control Modules 1204, recited in paragraph 0109) is adapted to allow the equalizer tap initialization module, the fine carrier estimation module (fig. 3, 260, "generate fine frequency correction and estimate, recited in paragraphs 0040-0042) and the fine frame synchronization module (fig. 4, Channel Compensation Module 330, recited in paragraph 0064-0065) to access the buffer (fig. 6, Memory Block, recited in paragraphs 0109-0110) responsive to receipt ("symbol data and preamble", recited in paragraphs 0064-0065) of at least a portion of a preamble ("first portion of an OFDM preamble", recited in paragraph 0018) by the OFDM receiver (fig. 6, OFDM receiver 1206, recited in paragraph 0109).

Regarding claim 11, a pilot carrier tracking module (fig. 5, Error Estimation Circuit Tone N 556, "pilot tone being processed", recited in paragraph 0073) that is adapted to receive data ("OFDM signal or data", recited in paragraph 0073) from the equalizer module (fig. 3, Frequency Correction Estimate 256, recited in paragraphs 0040-0045); a pilot frame tracking module ("frequency Error estimates per tone basis", recited in paragraph 0045) that is adapted to provide data ("resulting data being supplied", recited in paragraph 0045-0046) to the buffer (fig. 6, Memory Device 1204, recited in paragraph 0110-0111); and wherein the receiver controller (fig. 6, Control Modules 1204, recited in paragraph 0109) is adapted to activate the equalizer module (fig. 3, Frequency Correction Estimate 256, recited in paragraphs 0040-0045) the pilot carrier tracking module (fig. 5, Error Estimation Circuit Tone N 556, "pilot tone being processed", recited in paragraph 0073) and the pilot frame tracking module (fig. 5, Error Estimation Circuit Tone N 556, "pilot tone being processed", recited in paragraph 0073) responsive to the receipt of at least a portion of an OFDM signal ("first portion of an OFDM preamble", recited in paragraph 0018)l by the OFDM receiver (fig. 6, OFDM receiver 1206, recited in paragraph 0109).

Regarding claim 12, wherein the receiver controller (fig. 6, Control Modules 1204, recited in paragraph 0109, fig. 6, Receiver 1206, recited in paragraph 0109) is a state machine ("modules with machine with executable instructions", recited in paragraph 0110).

Regarding claim 20, a pilot carrier tracking module (fig. 5, Error Estimation Circuit Tone N 556, "pilot tone being processed", recited in paragraph 0073, "error

estimated generated from pilot tones", recited in paragraph 0019) that is adapted to receive data from the equalizer module (fig. 3, Frequency Correction Estimate 256, recited in paragraphs 0040-0045); a pilot frame tracking module (fig. 5, Error Estimation Circuits Tone N 556, "pilot tone being processed", recited in paragraph 0073, "error estimated generated from pilot tones", recited in paragraph 0019) that is adapted to provide data ("resulting data being supplied", recited in paragraph 0045-0046) to the buffer (fig. 6, Memory Block, recited in paragraphs 0109-0110); and wherein the device controller (fig. 6, Control Modules 1204 with processor 12010, recited in paragraph 0109) is adapted to activate the equalizer module, the pilot carrier tracking module (fig. 5, Error Estimation Circuits Tone N 556, "pilot tone being processed", recited in paragraph 0073, "error estimated generated from pilot tones", recited in paragraph 0019) and the pilot frame tracking module (fig. 5, Error Estimation Circuits Tone N 556, "pilot tone being processed", recited in paragraph 0073, "error estimated generated from pilot tones", recited in paragraph 0019) responsive to the receipt of a signal by the device (fig. 6, OFDM receiver 1206, recited in paragraph 0109).

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Dejonghe et al. with Nakai et al., Park et al, and Rafie et al., and Yamada et al. by using features as taught by Scarpa et al. in order to recover a carrier frequency (OFDM signals) so that transmission quality can be improved (See paragraphs 0011-0012 for motivation).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Korobkov et al (US 2007/0183308 A1), and Atungsiri et al(US 7,177,376 B2).

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CANDAL ELPENORD whose telephone number is (571)270-3123. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Bin Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Candal Elpenord/

Examiner, Art Unit 2416

/Kwang B. Yao/

Supervisory Patent Examiner, Art Unit 2416